

REMARKS

Claims 1-17 are now active in this application.

REJECTION OF CLAIMS UNDER 35 U.S.C. § 102 AND § 103

I. Claims 1-3, 6, 8 and 10-15 are rejected under 35 U.S.C. § 102(e) as being anticipated by Lau et al. (USPN 6,463,032), for the reasons substantially of record.

The rejections are respectfully traversed.

As noted in the 116 Amendment dated July 12, 2005, there is a significant difference between the claimed invention and the arrangement disclosed by Lau et al. that scotches the factual determination that Lau et al. identically describes the inventions of independent claims 1, 8 and 12.

Independent claim 1 requires, *inter alia*:

- a transmit queue queuing data retrieved from the memory for transmission from the port,
- an output terminal outputting the data packets, and
- a data path connecting the transmit queue and the output terminal, the data path having a gate controlling transferring of data packets in the data path to the output terminal.

Independent claim 8 requires, *inter alia*:

- reading data from the memory corresponding to each data packet to be transmitted from a respective transmit port and storing in a transmit queue from the respective port;
- transferring each data packet from the transmit queue to a data path connected between the transmit queue and an output terminal; and
- responsive to assertion and deassertion of an enable signal, transferring and blocking transferring data packets in the data path to the output terminal.

Independent claim 12 requires, *inter alia*:

a data path connecting between the transmit queue and the output terminal; and

logic coupled to the data path that selectively controls blocking of data from the transmit queue to the output terminal.

The Examiner asserted in the Office Action of March 16, 2005, as well as in the present Office Action, that “Lau discloses a plurality of output queues 58 for outputting data, and a data path between the output queues 58 for transmitting the data corresponding to the MAC port terminal to a FIFO of an identified output port.” In response, Applicants noted that output queues 58 are **NOT** the transmit queue recited in the claims and which is shown in Fig. 4 of the present application as Transmit FIFO 470. The data path 490 connects between transmit FIFO 470 and the outputting of the frame to RMII 18. The output queues 58 of the present application and of Lau et al. are the same and provide the same function of storing frame pointers, not data packets retrieved from the memory. The frame pointer is used to retrieve a data packet from the memory to be placed in an output queue, but is not a data packet.

The Examiner, in the Response to Arguments section of the present Office Action, refers to column 1, lines 25-42 in support of the assertion “that the ports, memory, transmit queue, output terminal and data path are all disclosed in Lau”. However, column 1, lines 25-42 is merely a general discussion of the disclosure of the invention and describes:

The invention provides a novel method of overflow data handling in a multiport data switching system having a decision making engine *for controlling data forwarding between receive ports and at least one transmit port*. Data blocks representing received data packets are placed in data queues corresponding to the receive ports. The data queues are transferred to logic circuitry for processing in accordance with a predetermined algorithm. Then, *a forwarding decision is made to determine the at least one transmit port*. An overflow bypass is provided to allow at least a portion of a data block to bypass the logic circuitry, when at least one of the data queues is in an overflow state.

In accordance with one aspect of the invention, each data block includes a pointer for indicating a memory location for storing the received data packet. The pointers are allowed to bypass the logic circuitry when the overflow state is detected. (Emphasis added)

A reasonable review of this portion clearly evinces that there is no description of a transmit queue, only of at least one transmit port, and the data queues mentioned are **NOT** transmit queues.

As noted further in the previous response, the description in Lau et al. of *a transmit queue* includes column 5, lines 1-18 and column 7, lines 45+ which describes the dequeuing logic 76 retrieving the frame data (from the SSRAM 36) for a particular output port *based on a fetched frame pointer and storing the frame data in the transmit FIFO*. Any data path in Lau et al. would connect between this transmit FIFO and MII 18. While a data path is inherently present in Lau et al., as the frame data stored in the transmit FIFO will be output to the MII 18, there is no disclosure of such data path and certainly no disclosure about a gate in the data path “controlling transferring of data packets in the data path to the output terminal” (claim 1), no disclosure about “transferring and blocking transferring data packets in the data path to the output terminal” ... “responsive to assertion and deassertion of an enable signal” (claim 8), and no disclosure about “logic coupled to the data path that selectively controls blocking of data from the transmit queue to the output terminal (claim 12)”.

As noted still further in the previous response, this is to be expected as Lau et al., having the same assignee as the present application, is **NOT** directed to a *bit bucket* as is the present application. What Lau et al. is directed to is a novel method of handling overflow in rules queues 102 which are part of IRC 40. Each rules queue is assigned to a single port and stores frame headers and pointers (not frame data) for each frame received at the port and the frame

header and pointer in each rules queue is used by forwarding descriptor generator 112 to produce a forwarding descriptor which includes the port vector and the frame pointer. The port vector is used to determine which one of the output queues 58 receives the frame pointer (not the frame data). The stored frame headers and pointers are output to forwarding descriptor generator 112 via ingress rules logic 106, source address lookup logic 108 and destination address lookup logic 110. The point of Lau et al. is to allow frame pointers to bypass ingress rules logic 106, source address lookup logic 108 and destination address lookup logic 110 and go directly to forwarding descriptor generator 112 when an overflow state of any of the rules queues 102 is detected, preventing the loss of data due to such overflow condition.

The Examiner's current response to such assertion is that "The Examiner agrees that Lau does not recite a bit bucket in the cited teachings, however, the claims also do not discuss a bit bucket. With regard to the gate, Lau does disclose AND gates used to allow and block certain portions of the transmitted data (see figure 5)".

Clearly, the Examiner misconstrues what Applicant intends in the above noted assertion regarding Lau. That is, Applicants asserted "this [difference] is to be expected as Lau et al., *having the same assignee as the present application*, is **NOT** directed to a *bit bucket* as is the present application. What Lau et al. is directed to is a novel method of handling *overflow in rules queues 102* which are part of IRC 40." By this assertion, Applicants are explaining why the above noted specific features of independent claims 1, 8 and 12 are not disclosed in Lau. That is, the phrase "bit bucket" is being used to describe what the claimed subject matter encompasses and since Lau does not disclose such a "bit bucket", it would not be expected to disclose the above noted specific features of independent claims 1, 8 and 12.

Figure 5 of Lau et al. shows overflow handling logic of the rules queue overflow handling system. The overflow handling logic does not change the natural manner in which the multiport switch of Lau et al. handles receipt and forwarding of frame data. More specifically, received frame data is placed into a receive FIFO buffer and is then transferred to SSRAM 36. The frame data is then retrieved from SSRAM 36 and transferred to a transmit FIFO buffer (i.e., a transmit queue). *The overflow handling logic disclosed in Lau et al. is clearly NOT involved with operations/functions in providing frame data in the transmit FIFO buffer to a (MAC) data path connecting between such transmit FIFO and the outputting of the frame to MII 18* (emphasis added).

More specifically, each of independent claims 1, 8 and 12 deals with a *data path connecting the transmit queue and the output terminal*. The data path connecting the transmit queue and the output terminal is a specific path and would correspond to a path in Lau et al. connecting between the transmit FIFO (described at column 5, lines 1-18 and column 7, lines 45+ of Lau) and MII 18. In this regard, the AND gates of figure 5 of Lau, which the Examiner refer to as the claimed gate of claim 1, have nothing to do with a *data path connecting the transmit queue and the output terminal* and, in fact, occur prior to the claimed *data path connecting the transmit queue and the output terminal*. Thus, reasonable interpretation of what is disclosed in Lau leads to the unassailable conclusion that the subject matter of figure 5 of Lau has nothing to do with the data path of independent claims 1, 8 and 12 connecting the transmit queue and the output terminal.

The above argued difference between the claimed system and method vis-à-vis the device and method of Lau et al. undermines the factual determination that Lau et al. identically describes the claimed inventions within the meaning of 35 U.S.C. § 102. *Minnesota Mining &*

Manufacturing Co. v. Johnson & Johnson Orthopaedics Inc., 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992); *Kloster Speedsteel AB v. Crucible Inc.*, 793 F.2d 1565, 230 USPQ 81 (Fed. Cir. 1986). Applicants, therefore, submit that the imposed rejection of independent claims 1, 8 and 12, as well as dependent claims 2, 3, 6, 8 and 10-15 under 35 U.S.C. § 102 for lack of novelty as evidenced by Lau et al. is not factually or legally viable and, hence, solicit withdrawal thereof.

II. Claims 4, 5, 7, 9, 16 and 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Lau et al. in view of Holden (USPN 6,151,301), for the reasons substantially of record.

The rejections are respectfully traversed.

As independent claims 1, 8 and 12 are patentable over Lau et al., claims 4, 5 and 7 depending directly or indirectly from claim 1, claim 9 depending from claim 8, and claims 16 and 17 depending indirectly from claim 12 are patentable over Lau et al. also, even when considered in view of Holden. Consequently, the allowance of claims 4, 5, 7, 9, 16 and 17 is respectfully solicited.

CONCLUSION

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, Examiner is requested to call Applicants' attorney at the telephone number shown below.

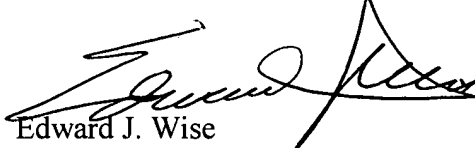
To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

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including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

A handwritten signature in black ink, appearing to read "Edward J. Wise", written over a horizontal line.

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